ABSTRACT

A method and system for determining wire capacitance for a VLSI circuit design, comprising determining all hierarchical blocks of a portion of the design; storing, for a plurality of the blocks, indicia of the most accurate one of a plurality of wire capacitance data sources; generating a wire capacitance database with an entry for each net in at least a plurality of the blocks, using information stored in at least one of the wire capacitance data sources; generating a hierarchical connectivity model for the design; and using the hierarchical connectivity model and said wire capacitance database to determine a cumulative wire capacitance value for each HLSN in each of the blocks in a portion of the design to be analyzed.